

- ☐ Home
- ☐ What Can I Access?
- ☐ Log-out

Tables of Contents

- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

Search

- ☐ By Author
- ☐ Basic
- ☐ Advanced

Member Services

- ☐ Join IEEE
- ☐ Establish IEEE Web Account

 Print Format

Your search matched **213** of **774948** documents.

Results are shown **25** to a page, sorted by **publication year** in **descending** order.

You may refine your search by editing the current search expression or entering a new one the text box.

Then click **Search Again**.

(ASIP or ASIC) and register

[Search Again](#)

Results:

Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

51 IP development and management of IP DB enabling efficient system-on-chip design

Young-ho Lee; Ki-Won Kwon; Jin-Tea Kim; Chul-Dong Lee

ASICs, 1999. AP-ASIC '99. The First IEEE Asia Pacific Conference on , 1999

Page(s): 229 -232

[\[Abstract\]](#) [\[PDF Full-Text \(304 KB\)\]](#) **CNF**

52 Implementation of a cycle-based simulator for the design of a processor core

Moon Gyung Rim; Byung In Moon; Sang Jun An; Dong Ryul Ryu; Yong Surk Lee

ASICs, 1999. AP-ASIC '99. The First IEEE Asia Pacific Conference on , 1999

Page(s): 108 -111

[\[Abstract\]](#) [\[PDF Full-Text \(396 KB\)\]](#) **CNF**

53 Cost/performance trade-off in floating-point unit design for 3D geometry processor

Cheol-Ho Jeong; Woo-Chan Park; Tack-Don Dan; Shin-Dug Kim

ASICs, 1999. AP-ASIC '99. The First IEEE Asia Pacific Conference on , 1999

Page(s): 104 -107

[\[Abstract\]](#) [\[PDF Full-Text \(540 KB\)\]](#) **CNF**

54 Power analysis of gated pipeline registers

Wu Ye; Irwin, M.J.

ASIC/SOC Conference, 1999. Proceedings. Twelfth Annual IEEE International , 1999
Page(s): 281 -285

[\[Abstract\]](#) [\[PDF Full-Text \(220 KB\)\]](#) [CNF](#)

55 A quadratic programming approach to clock skew scheduling for reduced sensitivity to process parameter variations

Kourtev, I.S.; Friedman, E.G.

ASIC/SOC Conference, 1999. Proceedings. Twelfth Annual IEEE International , 1999
Page(s): 210 -215

[\[Abstract\]](#) [\[PDF Full-Text \(364 KB\)\]](#) [CNF](#)

56 Practical scan test generation and application for embedded FIFOs

Rearick, J.

Test Conference, 1999. Proceedings. International , 1999
Page(s): 294 -300

[\[Abstract\]](#) [\[PDF Full-Text \(504 KB\)\]](#) [CNF](#)

57 A design and tool reuse methodology for rapid prototyping of application specific instruction set processors

Young Geol Kim; Tag Gon Kim

Rapid System Prototyping, 1999. IEEE International Workshop on , 1999
Page(s): 46 -51

[\[Abstract\]](#) [\[PDF Full-Text \(324 KB\)\]](#) [CNF](#)

58 On the use of pseudorandom sequences for high speed resource allocators in superscalar processors

Srinivasan, S.; John, L.K.

Computer Design, 1999. (ICCD '99) International Conference on , 1999
Page(s): 124 -130

[\[Abstract\]](#) [\[PDF Full-Text \(128 KB\)\]](#) [CNF](#)

59 Resource constrained dataflow retiming heuristics for VLIW ASIPs

Jacome, M.; de Veciana, G.; Akturan, C.
Hardware/Software Codesign, 1999. (CODES '99) Proceedings of the
Seventh International Workshop on , 1999
Page(s): 12 -16

[\[Abstract\]](#) [\[PDF Full-Text \(424 KB\)\]](#) [CNF](#)

60 **A two-state methodology for RTL logic simulation**
Bening, L.
Design Automation Conference, 1999. Proceedings. 36th , 1999
Page(s): 672 -677

[\[Abstract\]](#) [\[PDF Full-Text \(488 KB\)\]](#) [CNF](#)

61 **Common-case computation: a high-level technique for power and performance optimization**
Lakshminarayana, G.; Raghunathan, A.; Khouri, K.S.; Jha, N.K.; Dey, S.
Design Automation Conference, 1999. Proceedings. 36th , 1999
Page(s): 56 -61

[\[Abstract\]](#) [\[PDF Full-Text \(612 KB\)\]](#) [CNF](#)

62 **TAO-BIST: a framework for testability analysis and optimization of RTL circuits for BIST**
Ravi, S.; Jha, N.K.; Lakshminarayana, G.
VLSI Test Symposium, 1999. Proceedings. 17th IEEE , 1999
Page(s): 398 -406

[\[Abstract\]](#) [\[PDF Full-Text \(208 KB\)\]](#) [CNF](#)

63 **RTL power management**
Toomajian, G.
Wescon/98 , 1998
Page(s): 139 -146

[\[Abstract\]](#) [\[PDF Full-Text \(496 KB\)\]](#) [CNF](#)

64 **Low-power fully-testable flow meter in CMOS ASIC**
Calvo, O.; Roca, M.
Integrated Circuit Design, 1998. Proceedings. XI Brazilian Symposium on , 1998
Page(s): 171 -174

[\[Abstract\]](#) [\[PDF Full-Text \(40 KB\)\]](#) **CNF**

65 Test methodology for a microprocessor with partial scan

Day, L.L.; Ganfield, P.A.; Rickert, D.M.; Ziegler, F.J.

Test Conference, 1998. Proceedings., International , 1998

Page(s): 708 -716

[\[Abstract\]](#) [\[PDF Full-Text \(788 KB\)\]](#) **CNF**

66 Efficient high-speed CIC decimation filter

Kei-Yong Khoo; Zhan Yu; Wilson, A.N., Jr.

ASIC Conference 1998. Proceedings. Eleventh Annual IEEE

International , 1998

Page(s): 251 -254

[\[Abstract\]](#) [\[PDF Full-Text \(372 KB\)\]](#) **CNF**

67 Circuit techniques for high-speed and low-power multi-port SRAMs

Khellah, M.M.; Elmasry, M.I.

ASIC Conference 1998. Proceedings. Eleventh Annual IEEE

International , 1998

Page(s): 157 -161

[\[Abstract\]](#) [\[PDF Full-Text \(340 KB\)\]](#) **CNF**

68 Automated synthesis of a multiple-sequence test generator using 2-D LFSR

Xin Yuan; Chen, C.-I.H.

ASIC Conference 1998. Proceedings. Eleventh Annual IEEE

International , 1998

Page(s): 75 -79

[\[Abstract\]](#) [\[PDF Full-Text \(392 KB\)\]](#) **CNF**

69 Integrated scheduling and allocation of high-level test synthesis

Tianruo Yang; Zebo Peng

ASIC Conference 1998. Proceedings. Eleventh Annual IEEE

International , 1998

Page(s): 81 -87

[\[Abstract\]](#) [\[PDF Full-Text \(804 KB\)\]](#) **CNF**

70 An LPC cepstrum processor for speech recognition*In-Chul Hwang; Sung-Nam Kim; Young-Woo Kim; Soo-Won Kim*

Circuits and Systems, 1998. ISCAS '98. Proceedings of the 1998 IEEE International Symposium on , Volume: 4 , 1998

Page(s): 233 -236 vol.4

[\[Abstract\]](#) [\[PDF Full-Text \(260 KB\)\]](#) **CNF**

71 Implementing C designs in hardware: a full-featured ANSI C to RTL Verilog compiler in action*Soderman, D.; Panchul, Y.*

Verilog HDL Conference and VHDL International Users Forum, 1998. IVC/VIUF. Proceedings., 1998 International , 1998

Page(s): 22 -29

[\[Abstract\]](#) [\[PDF Full-Text \(600 KB\)\]](#) **CNF**

72 A performance maximization algorithm to design ASIPs under the constraint of chip area including RAM and ROM sizes*Nguyen Ngoc Binh; Imai, M.; Takeuchi, Y.*

Design Automation Conference 1998. Proceedings of the ASP-DAC '98. Asia and South Pacific , 1998

Page(s): 367 -372

[\[Abstract\]](#) [\[PDF Full-Text \(540 KB\)\]](#) **CNF**

73 Techniques for functional test pattern execution*Hong, I.; Potkonjak, M.*

Design Automation Conference 1998. Proceedings of the ASP-DAC '98. Asia and South Pacific , 1998

Page(s): 283 -288

[\[Abstract\]](#) [\[PDF Full-Text \(560 KB\)\]](#) **CNF**

74 PSCP: A scalable parallel ASIP architecture for reactive systems*Pyttel, A.; Sedlmeier, A.; Veith, C.*

Design, Automation and Test in Europe, 1998., Proceedings , 1998

Page(s): 370 -376

[\[Abstract\]](#) [\[PDF Full-Text \(188 KB\)\]](#) **CNF**

75 A 33 GB/s 13.4 Mb integrated graphics accelerator and frame buffer

Torrance, R.; Mes, I.; Hold, B.; Jones, D.; Crepeau, J.; DeMone, P.; MacDonald, D.; O'Connell, C.; Gillingham, P.; White, R.; Duggins, S.; Fielder, D.

Solid-State Circuits Conference, 1998. Digest of Technical Papers.

1998 IEEE International , 1998

Page(s): 340 -341, 461

[\[Abstract\]](#) [\[PDF Full-Text \(948 KB\)\]](#) **CNF**

[\[Prev\]](#) [1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [\[Next\]](#)

[Home](#) | [Log-out](#) | [Journals](#) | [Conference Proceedings](#) | [Standards](#) | [Search by Author](#) | [Basic Search](#) | [Advanced Search](#)
[Join IEEE](#) | [Web Account](#) | [New this week](#) | [OPAC Linking Information](#) | [Your Feedback](#) | [Technical Support](#) | [Email Alerting](#)
[No Robots Please](#) | [Release Notes](#) | [IEEE Online Publications](#) | [Help](#) | [FAQ](#) | [Terms](#) | [Back to Top](#)

Copyright © 2002 IEEE — All rights reserved